**Amendments to the Specification:**

Please revise the second full paragraph beginning on page 5, line 11, and continuing through to page 6, line 2, as follows:

A storage router is typically implemented as a single chip computer (or processor) with one or more internal busses, ~~such as~~ but one PCI busses. I/O controllers attached to these PCI busses connect to the storage interfaces. A memory controller attaches to the PCI bus to provide both the processor and the I/O controllers access to a central memory. In such a storage router system, parity may be generated by both the single chip computer and by the I/O controllers. Data sent across these PCI busses is verified so that no errors are introduced in the data as it is transferred. There is, however, no provision for data checking within the I/O controllers or processor, or through the memory controller. If a hardware failure occurs in the I/O controllers, the memory controller, or the processor, it is possible for data being transferred through the storage router to be corrupted, without detection.

Please delete the first full paragraph (i.e., the paragraph beginning with "FIGURE 2") beginning on page 6, line 4; and please add the following paragraph at page 12, line 1, as follows:

FIGURE 2 shows a block diagram of a typical storage router 200, where storage router 200 is similar to computer system 100 shown in FIGURE 1, but in addition to a first PCI bus 214a, it has a second PCI bus 214b. Memory space 206 is accessible via memory controller 204 through both of the PCI busses 214a, 214b. The processor 202 is typically an integrated device that contains dual PCI interfaces 214a, 214b and an internal memory controller 204, which controls a second memory area. The storage router also provides additional storage interfaces 210a, 210b, 220a, 220b, some of which are attached to host systems 222 rather than to storage devices (e.g., disk drives 166, etc.).